IQ-VIN – High Performance Video Input

Description

IQ-VIN is a high performance video input, designed to support high-performance applications, with resolutions larger than full HD 1080p (up to 2048x2048) and stable operation in SoCs with limited memory bandwidth.

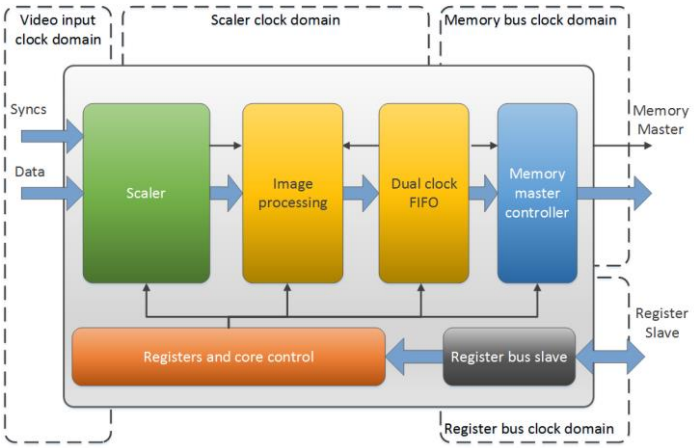
The IP Core accepts digital RGB or YUV video data, output from a HDMI 1.3/1.4a decoder, DisplayPort, HD-SDI, or other video reception interface.

IQ-VIN Integrates the IQ-ScalR video scaler IP, enabling frame-by-frame image scaling. Upscaling and downscaling are supported, independently for horizontal and vertical axis. Scaled images are outputted to memory in bursts with maximum efficiency.

Integrated image processing allows the color depth do be reduced from 24bpp pixels to 16bpp using dithering to achieve high image quality, while significantly reducing the required memory bandwidth.

The bus architecture and scaler parameters are configurable at compile time, offering a trade-off between image quality/bus performance and resource consumption.

Block Diagram



Implementation

Lattice (ECP3-35EA)

LUT4s	Regs	EBRs	Multip.	F_{max}	IO Pins
2820	2807	20	24	158 MHz *	193 **

* Maximum frequency of the system bus interface, for AMBA AHB

** Assuming all core ports routed off-chip

Verification

The core has been rigorously tested in functional simulation and actual hardware.

The core is accompanied with an automated testbench with an image source simulation model and a memory simulation model.

The memory model can dump content to a file, allowing analysis of the simulation results through simple software provided with the model.

Features

- Support for resolutions up to 2048x2048
- Support for YUV or RGB color input
- Support for 16bpp (5:6:5) or 24 bit RGB output color depth.
- Vertical and horizontal cropping of the input image.
- Reduction of colordepth from 24-bit on input to 16-bit in memory with dithering.
- Configurable width of the scaler interpolation filter.
- Frame by frame image scaling, independent scaling factors for X and Y axes.
- Complete separation of all IP clock domains, allowing the fastest clocks to be used only in the scaler, separating them from the system bus clocks (set by the SoC requirements).
- Downscaling limited by scaler resolution, upscaling limited only by the ratio between the input pixel frequency (defined by the video source) and the scaler clock frequency (defined in SoC)
- High-throughput design with deep pixel buffers, allowing for the robust stable behavior even on the busiest system buses.
- Frame sync output, frame skip support
- Integrated DMA memory master supporting low-overhead burst transfers
    - Master bus interfaces
        - AMBA (AHB | AXI4)
        - Avalon
        - Peregrine*

* Peregrine bus is Mikroprojekt's proprietary bus architecture, optimized for FPGA Implementations

- Configuration bus slave interface with address-mapped registers
    - Slave bus interfaces
        - AMBA APB
        - Avalon

Applications

- Digital Signage
- Video monitors
- TVs, Set-Top Boxes
- Automotive infotainment
- Medical instrumentation
- Visualization Systems
- Human Machine Interface (HMI) Systems

Deliverables

- Precompiled IP core in desired configuration or encrypted IP core RTL
- Testbench
- Datasheet
- User manual
- Implementation guide

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